



# UNITED STATES PATENT AND TRADEMARK OFFICE

*cel*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,571	10/23/2000	Ryszard Bleszynski	40291/2000100	1452

7590 06/29/2005

Wilson & Ham  
PMB 348  
2530 Berryessa Road  
San Jose, CA 94566

EXAMINER

HAN, CLEMENCE S

ART UNIT PAPER NUMBER

2665

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/035,571

Applicant(s)

BLESZYNSKI ET AL.

Examiner

Clemence Han

Art Unit

2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,3-10,12-31,33-41,43-48 and 50-57 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 17-31,33-41,43-48 and 50-57 is/are allowed.
- 6) ☒ Claim(s) 1,3-10 and 12-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1, 3-10 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,415,366) in view of Foster (US 5,948,081).

In regarding to claim 1, Chen teaches a method to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels (See Figure 3), comprising: determining at least one load value of each of the plurality of memory channels (Column 3 Line 56-62); and based on the determined at least one load value, selecting a particular one of the plurality of memory channels (Column 2 Line 36-39). Chen, however, does not teach the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each

of the plurality of memory channels, the number of pending read requests. Foster teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, the number of pending read requests (Column 7 Line 28-30 and Line 59-61). It would have been obvious to one skilled in the art to modify Chen to use the number of pending read request as taught by Foster in order to improve memory bandwidth (Column 2 Line 36-38).

In regarding to claim 3, Foster teaches the step of selecting the particular one of the plurality of memory channels includes selecting the particular one of the plurality of memory channels that has a lowest number of pending read requests (Column 7 Line 28-30 and Line 59-61).

In regarding to claim 4, Chen teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending write requests, and the number of active buffers which is the number of a particular one of the plurality of buffers that is unavailable and corresponds to the particular one of the plurality of memory channels in each of the plurality of memory (Column 3 Line 56-62).

In regarding to claim 5, Chen teaches the step of selecting the particular one of the plurality of memory channels includes selecting the particular one of the plurality of memory channels that has at least one of a lowest number of pending write requests, a lowest number of active buffers, and a corresponding channel identification number that is next in a round robin scheme (Column 2 Line 36–39).

In regarding to claim 6, Chen teaches the memory unit as a plurality of dynamic random access memory units (Column 3 Line 26–28).

In regarding to claim 7, Chen teaches each of the plurality of buffers having a fixed-size (Column 3 Line 10–25).

In regarding to claim 8, Chen teaches receiving an incoming information element; if the size of the information element is greater than the fixed-size of each of the plurality of buffers, dividing the information element into a plurality of information element segments, each of the plurality of information element segments having a size less than or equal to the fixed-size of each of the at least one buffer (Column 3 Line 10–25); and storing at least one of the information element and a particular one of the plurality of information element segments within a particular one of the plurality of buffers corresponding to the selected one of the plurality of memory channels at a particular one of the plurality of memory lines (Column 3 Line 10–25).

In regarding to claim 9, Chen teaches each of the plurality of memory channels having a width equal to a width of the memory unit divided by the number of the plurality of memory channels (Figure 3, Column 3 Line 36).

In regarding to claim 10, Chen teaches a method to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels, comprising: determining at least one load value of each of the plurality of memory channels (Column 3 Line 56–62); and selecting a particular one of the plurality of memory channels that has a particular one of the at least one load value that is the lowest (Column 2 Line 36–43). Chen, however, does not teach the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending read requests and the number of pending write requests. Foster teaches the step of determining the at least one load value of each of the plurality of memory channels includes determining, for each of the plurality of memory channels, at least one of the number of pending read requests and the number of pending write requests

(Column 7 Line 28-30 and Line 59-61). It would have been obvious to one skilled in the art to modify Chen to use the number of pending read request as taught by Foster in order to improve memory bandwidth (Column 2 Line 36-38).

In regarding to claim 12, Chen teaches the step of selecting the particular one of the plurality of memory channels that has the lowest determined load includes selecting the particular one of the plurality of memory channels that has at least one of a lowest number of pending read requests and a lowest number of pending write requests (Column 2 Line 36-39).

In regarding to claim 13, Chen teaches the memory unit as a plurality of dynamic random access memory units (Column 3 Line 26-28).

In regarding to claim 14, Chen teaches each of the plurality of buffers having a fixed-size (Column 3 Line 10-25).

In regarding to claim 15, Chen teaches receiving an incoming information element; if the size of the information element is greater than the fixed-size of each of the plurality of buffers, dividing the information element into a plurality of information element segments, each of the plurality of information element segments having a size less than or equal to the fixed-size of each of the at least one buffer (Column 3 Line 10-25); and storing at least one of the information element and a particular one of the plurality of information element segments

within a particular one of the plurality of buffers corresponding to the selected one of the plurality of memory channels at a particular one of the plurality of memory lines (Column 3 Line 10-25).

In regarding to claim 16, Chen teaches each of the plurality of memory channels having a width equal to a width of the memory unit divided by the number of the plurality of memory channels (Figure 3, Column 3 Line 36).

*Allowable Subject Matter*

3. Claim 17-31, 33-41, 43-48 and 50-57 are allowed.

*Conclusion*

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will

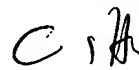



be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Clemence Han

  
STEVEN NGUYEN  
PRIMARY EXAMINER